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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,123	11/20/2003	Zachary Steven Smith	200209692-1	9105

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EXAMINER	
MEHRMANESH, ELMIRA	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,123	SMITH ET AL.	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The application of Smith et al., for a "Systems and methods for verifying core determinacy" filed November 20, 2003, has been examined.

Claims 1-25 are presented for examination.

Claims 16-21 are rejected under 35 USC § 101.

Claims 1-25 are rejected under 35 USC § 102.

Claim 16 is rejected under 35 USC § 112.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 16-21 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

As per claims 16-21, the limitation "computer-readable medium" is not limited to tangible embodiments. In view of Applicant's disclosure the medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., specification, page 17, line 24, electronic) and intangible embodiments (e.g., specification, page 17, magnetic, optical). As such, the claim is not limited to statutory subject matter and is therefore non-statutory.

Furthermore the limitations "system" with "logic configured to" is directed to non-statutory subject matter. Computer programs claimed as computer listings per se, i.e., the descriptions or expressions of the programs are not physical "things." They are

neither computer components nor statutory processes, as they are not "acts" being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer, which permit the computer program's functionality to be realized.

However examiner suggests a change of "a determinacy checker stored on a computer-readable medium" to "a determinacy checker with logic stored on a computer-readable medium".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 16 recites the limitation "system" in line 1. There is insufficient antecedent basis for this limitation in the claim. Examiner suggests a change of the limitation of "system" to "determinacy checker".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Mandyam et al. (U.S. Patent No. 5,928,334).

As per claim 1, Mandyam discloses a method for verifying core determinacy (Fig. 1), the method comprising:

extracting data stored in core model structures (col. 6, lines 57-65)

comparing the extracted data of one modeled processor core with extracted data of another modeled processor core (Fig. 1, element 110)

determining if any mismatching data will cause core divergence (col. 13, lines 22-36)

facilitating notice of an error if any mismatching data will cause core divergence (col. 9, lines 14-16) and (Figs. 10A-10C).

As per claim 2, Mandyam discloses extracting data comprises extracting data from core data storage and interconnect elements (col. 8, lines 15-20).

As per claim 3, Mandyam discloses extracting data comprises extracting data from at least one of core buffers, core caches, core queues, core state variables, core state machines, and bus values (col. 9, lines 40-47).

As per claim 4, Mandyam discloses determining comprises accessing a data structure that matches divergence results with given mismatched data (Fig. 14) and (col. 8, lines 46-49).

As per claim 5, Mandyam discloses determining comprises implementing an algorithm that uses the mismatched data as inputs (col. 10, lines 33-40).

As per claim 6, Mandyam discloses facilitating notice comprises pending a check (Fig. 13, BNE SYNC _ERROR) for a lockstep block checker to signal when divergence occurs (col. 12, lines 57-67).

As per claim 7, Mandyam discloses facilitating notice comprises flagging an error (col. 9, lines 14-16) if the lockstep block checker does not signal that divergence occurred (col. 8, lines 30-45).

As per claim 8, Mandyam discloses determining if a modeled processor is operating in lockstep mode (col. 12, lines 57-67).

As per claim 9, Mandyam discloses determining if a modeled processor is operating in lockstep mode comprises analyzing at least one of a lockstep block and a lockstep block checker (Fig. 16).

As per claim 10, Mandyam discloses a system for verifying core determinacy (Fig. 1), the system comprising:

means for determining if a modeled processor is operating in a lockstep mode (col. 13, lines 22-36)

means for extracting data stored in core model structures (col. 6, lines 57-65)

means for comparing the extracted data to determine if any data associated with one processor core does not match data associated with another processor core (Fig. 1, element 110)

means for determining if any mismatching data will cause core divergence (col. 9, lines 14-16) and (Figs. 10A-10C).

As per claim 11, Mandyam discloses the means for determining if a modeled processor is operating in a lockstep mode comprise means for analyzing at least one of a lockstep block and a lockstep block checker (col. 12, lines 57-67).

As per claim 12, Mandyam discloses means for extracting data comprise means for extracting data from core data storage and interconnect elements (col. 8, lines 15-20).

As per claim 13, Mandyam discloses means for determining if any mismatching data will cause core divergence comprise at least one of a data structure (col. 6, lines 57-65) and an algorithm (col. 10, lines 33-40).

As per claim 14, Mandyam discloses means for pending a check (Fig. 13, BNE SYNC _ERROR) for a lockstep block checker to signal when divergence occurs (col.

12, lines 57-67).

As per claim 15, Mandyam discloses means for flagging an error (col. 9, lines 14-16) and (col. 8, lines 30-45).

As per claim 16, Mandyam discloses a determinacy checker (Fig. 1, element 106), stored on a computer-readable medium (Fig. 1) the system comprising:

logic configured to determine if a modeled processor is operating in a lockstep mode (col. 13, lines 22-36)

logic configured to extract data stored in core model structures (col. 6, lines 57-65)

logic configured to compare the extracted data (Fig. 1, element 110)

logic configured to determine if any data associated with one processor core does not match data associated with another processor core (Fig. 12) and (col. 13, lines 22-36)

logic configured to determine if any mismatching data will cause core divergence (col. 13, lines 22-36)

logic configured to facilitate notification of an error if any mismatching data will cause core divergence (col. 9, lines 14-16) and (Figs. 10A-10C).

As per claim 17, Mandyam discloses logic configured to determine if a modeled processor is operating in a lockstep mode comprises logic configured to analyze at least

one of a lockstep block and a lockstep block checker (Fig. 16).

As per claim 18, Mandyam discloses logic configured to extract data comprises logic configured to extract data from core data storage and interconnect elements (col. 8, lines 15-20).

As per claim 19, Mandyam discloses logic configured to determine if any mismatching data will cause core divergence (col. 13, lines 22-36) comprises logic configured to access at least one of a data structure that matches divergence results with given mismatched data (col. 6, lines 57-65) and an algorithm that uses the mismatched data as inputs (col. 10, lines 33-40).

As per claim 20, Mandyam discloses logic configured to facilitate notification comprises logic configured to pend a check (Fig. 13, BNESYNC _ERROR) for a lockstep block checker to signal when divergence occurs (col. 12, lines 57-67).

As per claim 21, Mandyam discloses the logic configured to facilitate notification comprises logic configured to flag an error (col. 9, lines 14-16) and (col. 8, lines 30-45).

As per claim 22, Mandyam discloses a computer system (Fig. 1), comprising:

a processing device (Fig. 2A, elements P0, P1)

and memory (Fig. 1) including a determinacy checker (Fig. 1, element 106) that is configured to extract data stored in core model structures (col. 6, lines 57-65) compare the extracted data (Fig. 1, element 110), determine if any mismatching data will cause core divergence (col. 13, lines 22-36)

and facilitate notification of an error if the mismatching data will cause core divergence (col. 9, lines 14-16) and (Figs. 10A-10C).

As per claim 23, Mandyam discloses checker is configured to extract data from core data storage and interconnect elements (col. 8, lines 15-20).

As per claim 24, Mandyam discloses checker is configured to pend a check (Fig. 13, BNE SYNC _ERROR) for a lockstep block checker to signal when divergence occurs (col. 12, lines 57-67).

As per claim 25, Mandyam discloses checker is configured to flag an error (col. 9, lines 14-16) and (col. 8, lines 30-45).

Related Prior Art

The following prior art is considered to be pertinent to applicant's invention, but nor relied upon for claim analysis conducted above.

Maly et al. (U.S. PGPUB No. 20050154573), "Systems and methods for initializing a lockstep mode test case simulation of a multi-core processor design".

Kodaira (U.S. Patent No. 5,805,867), "Multi-processor simulation apparatus and method".

Griffin et al. (U.S. PGPUB No. 20020152418), "Apparatus and method for two computing elements in a fault-tolerant server to execute instructions in lockstep".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).